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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,784	04/04/2001	Jiin Lai	JCLA6095	4086
7590 06/10/2004 J.C. Patents, Inc. 4 VENTURE			EXAMINER	
			PHAN, RAYMOND NGAN	
SUITE 250			ART UNIT	PAPER NUMBER
Irvine, CA 926	018		2111	
			DATE MAILED: 06/10/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

: • • • • • • • • • • • • • • • • • • •		Application No.	Applicant(s)	- B			
		09/826,784	LAI ET AL.				
•	Office Action Summary	Examiner	Art Unit				
		Raymond Phan	2181				
Period fo	The MAILING DATE of this communication ap or Reply	ppears on the cover sheet	with the correspondence address	; 			
THE - Extermination of the control	ORTENED STATUTORY PERIOD FOR REPL MAILING DATE OF THIS COMMUNICATION. In second of the major of the major of the communication. In period for reply specified above is less than thirty (30) days, a reply period for reply is specified above, the maximum statutory period re to reply within the set or extended period for reply will, by staturely received by the Office later than three months after the mailing patent term adjustment. See 37 CFR 1.704(b).	136(a). In no event, however, may ply within the statutory minimum of t d will apply and will expire SIX (6) M te, cause the application to become	a reply be timely filed hirty (30) days will be considered timely. ONTHS from the mailing date of this communi ABANDONED (35 U.S.C. § 133).	cation.			
1)	Responsive to communication(s) filed on	·					
2a) <u></u> ☐	This action is FINAL . 2b) ☐ T	his action is non-final.					
3)□ Disposit	Since this application is in condition for allow closed in accordance with the practice unde ion of Claims	vance except for formal m r <i>Ex parte Quayle</i> , 1935 (natters, prosecution as to the me C.D. 11, 453 O.G. 213.	rits is			
4)⊠	Claim(s) 1-20 is/are pending in the application	on.					
	4a) Of the above claim(s) is/are withdra	awn from consideration.					
5)⊠	Claim(s) 8-12 is/are allowed.						
6)⊠	6)⊠ Claim(s) <u>1 and 13</u> is/are rejected.						
7)🖂	7)⊠ Claim(s) <u>2-7 and 14-20</u> is/are objected to.						
8)[Claim(s) are subject to restriction and/	or election requirement.					
Applicat	ion Papers	•					
<i>,</i> —	The specification is objected to by the Examin						
10)	The drawing(s) filed on is/are: a)□ acc	epted or b) objected to b	y the Examiner.				
	Applicant may not request that any objection to t						
11)	The proposed drawing correction filed on		disapproved by the Examiner.				
_	If approved, corrected drawings are required in r						
12)	The oath or declaration is objected to by the E	Examiner.					
-	under 35 U.S.C. §§ 119 and 120						
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).							
a)	☐ All b)☐ Some * c)☐ None of:						
	1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No							
* (3. Copies of the certified copies of the pri application from the International B See the attached detailed Office action for a list	Bureau (PCT Rule 17.2(a)).	е			
14)[]	Acknowledgment is made of a claim for domes	stic priority under 35 U.S.	C. § 119(e) (to a provisional appl	lication).			
	a) The translation of the foreign language p Acknowledgment is made of a claim for dome						
Attachmer	nt(s)						
2) Notice	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449) Paper No(s)	5) Notice	ew Summary (PTO-413) Paper No(s) of Informal Patent Application (PTO-152				
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Part III DETAILED ACTION

Notice to Applicant(s)

- 1. This application has been examined. Claims 1-20 are pending.
- 2. The Group and/or Art Unit location of your application in the PTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Group Art Unit 2181.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 1 and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu et al. (US No. 6,263,397) in view of Chen et al. (US No. 6,301,630).

In regard to claim 1, Wu et al. disclose the processing method of supporting message signaled interrupt to a chipset which is coupled to the PCI bus and system memory (see figure 2, col. 2, line 64 through col. 3, line 29) comprising the step of monitoring a memory write transaction on the PCI bus (see col. 6, lines 10-41). But Wu et al. do not specifically disclose the step of performing an interrupt sequence when an address of the memory write transaction falls into a reserved interrupt address; wherein the reserved interrupt address is located in an address of the system memory. However Chen et al. disclose the step of performing an interrupt sequence when an address of the write transaction falls into an address

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associated with selected buffer (see col. 14, lines 26-50). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Chen et al. within the system of Wu et al. because it would improve the interrupt response time and increase opportunities for combining or merging transaction in the buffer pool.

In regard to claim 13, Wu et al. disclose the processing method of supporting message signaled interrupt to a chipset which is coupled to the PCI bus and system memory (see figure 2, col. 2, line 64 through col. 3, line 29) comprising a DRAM controller coupled to the DRAM 130 (see col. 3, lines 19-30); CPU coupled to the chipset (see col. 3, lines 19-30). Wu et al. explicitly disclose the interrupt controller to generate the interrupt request signal to the CPU and enable the CPU to initiate the interrupt service routine (see col. 6, lines 11-41); interrupt delivery mechanism to monitor the memory write transaction on the (see col. 6, lines 10-41). But Wu et al. do not specifically disclose the step of performing an interrupt sequence when an address of the memory write transaction falls into a reserved interrupt address; wherein the reserved interrupt address is located in an address of the system memory. However Chen et al. disclose the step of performing an interrupt sequence when an address of the write transaction falls into an address associated with selected buffer (see col. 14, lines 26-50); message signal is generated to enable the interrupt controller to generate the interrupt request signal (see col. 14, line 50 through col. 15, line 65). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Chen et al. within the system of Wu et al. because it would improve the interrupt response time and increase opportunities for combining or merging transaction in the buffer pool.

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Allowable Subject Matter

5. Claims 8-12 are allowable over the prior of records.

6. The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claim 8-12 is allowable over the prior art of record because the Examiner found neither prior art cited in its entirety, nor based on the prior art, found any motivation to combine any of the said prior arts which teach a message signaled interrupt calculator, coupled to the message signal interrupt detector and the CPU interface to receive and count the message signaled interrupt acknowledging signal and to form an interrupt counting value, converting the interrupt counting value into a sent interrupt counting value, and outputting the sent interrupt counting value.

The remaining claims, not specifically mentioned, are allowed for same rationale from the parent claim by dependency

- 7. Claims 2-7, 14-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 8. The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claims 2-7 and 14-20 are allowable over the prior art of record because the Examiner found neither prior art cited in its entirety, nor based on the prior art, found any motivation to combine any of the said prior arts which teach the step of adding an interrupt counting value after the system specified message is written into the system memory and generating an interrupt request to the central processing unit according to the interrupt counting value (claim 2); a message signaled interrupt calculator, coupled to the message signaled interrupt

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detector and the CPU to receive and count the message signaled interrupt acknowledging to form an interrupt counting value and to convert the interrupt counting value into a sent interrupt counting value, and to output the sent interrupt counting value according to the mother board interface; and a message signaled interrupt generator to generate the message interrupt request signal to the interrupt controller according to the interrupt counting value (claim 14).

The remaining claims, not specifically mentioned, are allowed for same rationale from the parent claim by dependency

Conclusion

- 9. Claims 1 and 13 are rejected. Claims 2-7 and 14-20 are objected. Claims 8-12 are allowed.
- 10. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Jayakumar et al. (US No. 6,021,458) disclose a method and apparatus for handling multiple level/triggered and edge-triggered interrupts.

Waldron et al. (US No. 6,253,275) disclose an interrupt gating method for PCI bridges.

Chang et al. (US No. 5,835,779) disclose a message transmission among processing units using interrupt control technique.

Haren et al. (US No. 6,192,442) disclose an interrupt controller.

Seeman (US No. 5,881,253) discloses a computer system using posted memory write buffers in a bridge to implement system management mode.



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Tetrick (US No. 6,006,301) discloses a multi-delivery scheme interrupt router.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (703) 306-2756. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (703) 305-9656 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (703) 872-9306.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [raymond.phan@uspto.gov].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Raymond Phan

11/19/03